CLAIMS

What is claimed is:

1. An memory controller comprising:

a memory enable deassertion delay (MEDD) logic to set a wait period for the deassertion of a memory enable signal after completion of a memory operation, the wait period chosen for a preferred latency versus power savings tradeoff; and

the memory enable signal used when reading from and writing to the memory.

2. The memory controller of claim 1, wherein the memory comprises double data rate (DDR) dynamic random access memory (DRAM).

3. The memory controller of claim 1, wherein a setting for reading is different from the setting for writing to the memory.

4. The memory controller of claim 1, wherein the MEDD is set using a counter.

5. The memory controller of claim 4, wherein the counter is a programmable counter.

6. The memory controller of claim 4, wherein the counter is a one-time programmable counter.

7. A method comprising:

testing an integrated circuit; and

setting a variable memory enable signal de-assertion (MEDD) wait time based on a preferred latency versus power savings tradeoff; and

using the memory enable signal to enable reading from and writing to a memory.

8. The method of claim 7, wherein the variable MEDD is set once, during an initial testing of a chipset.

9. The method of claim 7, wherein the variable MEDD may be adjusted during use.

10. The method of claim 7, further comprising:

during basic input-output system (BIOS) boot-up of the computer system, setting the MEDD.

11. An apparatus comprising:

a memory controller to provide access to a memory for reading and writing using a variable duration CKE signal;

the variable duration CKE signal to be asserted for access to the memory, the variable duration CKE signal set based on a preferred latency versus power savings tradeoff.

12. The apparatus of claim 11, further comprising:

a programmable memory to store a delay before deassertion of the CKE signal, making the CKE signal a variable signal.

13. The apparatus of claim 12, wherein the programmable memory is an erasable programmable read-only memory.

14. The apparatus of claim 11, wherein the programmable memory comprises a programmable counter.

15. The apparatus of claim 12, further comprising:

a basic input-output system (BIOS) to load the delay from the programmable memory into the computer system.

16. The apparatus of claim 11, wherein the memory is dual data rate dynamic random access memory (DDR DRAM).

17. A computing system comprising:

a means for moving a memory from stand-by status to active status to enable an operation to be completed on the memory; and

a programmable means for setting a delay before returning the memory to the stand-by status.

18. The computing system of claim 17, wherein the programmable means comprises a one-time programmable means.

19. The computing system of claim 18, wherein the programmable means comprises a reprogrammable means.

20. A system comprising:

dual data rate dynamic random access memory (DDR DRAM);

a programmable register;

a memory enable deassertion delay (MEDD) logic to set the programmable register to set a wait period for the deassertion of a memory enable signal after completion of a memory operation; and

the memory enable signal used when reading from and writing to the DDR DRAM.

21. The system of claim 20, further comprising:

a MEDD configuration bit to alter the MEDD.

22. The system of claim 20, further comprising:

a basic input-output system (BIOS) to load the delay from the programmable memory into the computer system.